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VASAVI COLLEGE OF ENGINEERING (Autonomous), HYDERABAD B.E. (CSE: CBCS) III-Semester Main Examinations, December-2017

Logic & Switching Theory

Time: 3 hours

Max. Marks: 70

Note: Answer ALL questions in Part-A and any FIVE from Part-B

Part-A $(10 \times 2 = 20 \text{ Marks})$

- 1. Simplify the given function $f=(A+(BC)^1)^1(AB^1+ABC)$
- 2. Determine the Sum of Minterms form for $F(x,y,z)=x^1y+z^1+xyz$
- 3. Implement EX-NOR gate using only NOR gates.
- 4. Implement the following Boolean function with NAND-NAND logic. $F(A,B,C)=\sum(0,1,3,5)$
- 5. Implement the following Boolean function using 4:1 multiplexer. F(A,B,C)= $\sum(1,3,5,6)$
- 6. Design a combinational logic circuit with three input variables that will produce a logic1 output when more than one input variables are logic1.
- 7. Compare Synchronous & Asynchronous Sequential Circuits.
- 8. Draw the logic diagram, logic symbol and Truth table of JK Flip flop.
- 9. Design a combinational circuit using ROM that accepts a 3-bit number and outputs a binary number equal to the square of the input number.
- 10. Draw the structure of PLA.

Part-B $(5 \times 10 = 50 \text{ Marks})$

11. a) Prove using De-Morgans theo	orem that XOR and XNOR are complement to each other.	[5]
b) Convert the following equation $Y = (A+B)(A+C)(B+C^{1}).$	on into the standard POS form.	[5]
12. a) Simplify the following function $F(A,B,C,D) = \sum m(0,1,2,3,4)$	on and find essential prime implicants. ,6,8,9,10,11)	[6]
b) Implement Y=AC+BC+AB+	D with NOR-NOR logic.	[4]
13. a) Design a 2 to 4 decoder using	, NOR gates only.	[5]
b) Design a circuit with three inp the binary count of the number	puts (A, B, C) and 2 outputs (X, Y), where the outputs are er of "ON" (HIGH) inputs.	[5]
14. a) Design a sequence detector for	or the sequence 10110. Use JK Flip-Flop.	[6]
b) Show how a JK flip flop can	be constructed using a T flip flop and other logic gates.	[4]
15. a) Derive the PLA program table Minimize the number of prod	le for a combinational circuit that squares a 3-bit number. luct terms.	[5]
b) Construct a 128×8 ROM wi connections and a decoder.	th four 32×8 ROM chips with an enable input, external	[5]

		Code No. : 13206		
1	16. a) Find the complement of $f=A+[(B+C^1).D+E^1]F$.		[4]	
	b) Express the following functions in sum of min terms and product of max terms.		[6]	
	i) $F(A,B,C) = 1$ ii) $F(A,B,C) = (AB+C) (B+AC)$		[~]	
1	7. Answer any <i>two</i> of the following:			
	a) Explain the design procedure for combinational circuits.		[5]	
	b) Design a 3-bit UP/DOWN counter which counts up when the control signal M=1 and counts down when M=0.		[5]	
	c) Write short notes on Programmable Array Logic.		[5]	
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	b) Design a circuit with three inputs (A, B, C) and 2 couples (X, Y), where the compare net- the binary used of the number of "ON" (IIIGH) inputs			
	b) Show how a JK file flop can be constructed using a T flop flop and other logic gates			